LVDS-LVPECL-CMOS Differential Oscillator 20MHz to 300MHz

FEATURES

- **LVDS - LVPECL - CMOS outputs available**
- **Low phase noise - Low phase jitter**
- **Internal 0.01µF SMD decoupling capacitor option**
- **Low Allen deviation**
- **High Frequency Fundamental Mode Crystal**
- **Extended Industrial temperature range**

DESCRIPTION

The DFXO series, 7 x 5mm SMD differential output oscillator is designed for applications requiring low jitter and ultra high frequency differential poutputs in a small footprint. Offered at frequencies from 20MHz to 300MHz with operation over a wide temperature range (-40° to +105°C). No external decoupling capacitor is required with optional internal capacitor. Designed and manufactured in USA by Statek Inc.

APPLICATIONS

Military & Aerospace

- **Avionics**
- **Communications**
- **Networking**

SPECIFICATION

Frequency Range:	20MHz to 300MHz
Supply Voltage[1]:	+3.3Volts ±10% (+2.5V ±10% available)
Operating Temperature:	-40° to +85°C
Shock, survival:	5,000g 0.3ms, ½ sine
Vibration, Survival:	20g, 10-2000Hz swept sine

ABSOLUTE MAXIMUM RATINGS

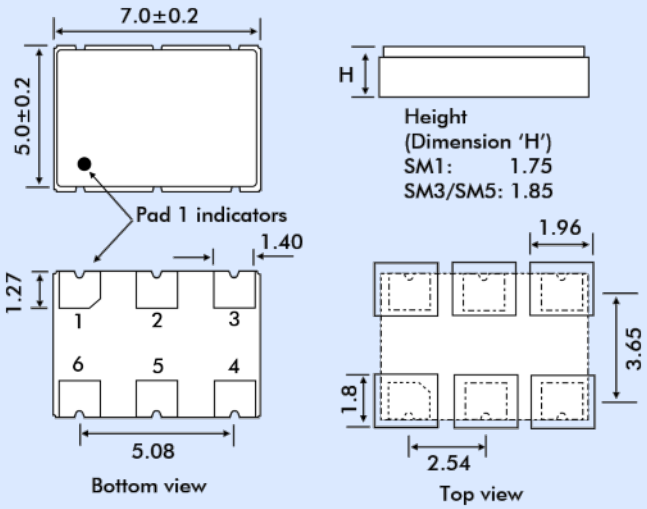
Supply Voltage V_{DD}:	-0.5Volts to 1.6 Volts
Storage Temperature:	-65° to +150°C
Maximum Process Temperature:	260°C for 10 seconds

ESD Protection Human Body Model 2kV.

TERMINATIONS

Designation	Termination
SM1	Gold Plated (Pb Free)
SM3	Solder dipped
SM5	Solder dipped (Pb Free)

OUTLINE & DIMENSIONS



Pad Connections
1 Enable/Disable or not connected (N)
2 (NC) Not Connected
3 Ground
4 LVDS - LVPECL - CMOS
5 LVDS - LVPECL (complementary)
6 Supply Voltage (V_{DD})

PACKAGING OPTIONS

DFXO: Tray Pack
Tape and Reel per EIA 481

ENABLE/DISABLE OPTIONS (T/N)

There are two Enable/Disable options, T and N. THe 'T' version has a Tri-state output and continues to oscillate internally when the output is put into the High Z state. As a result, when re-enabled, the oscillator does not have to restart and output with a stable frequency resumes almost immediately. The 'N' version does not have PIN 2 connected internally and so has no enable/disable function. The following table describes the Enable/Disable option 'T'.

	ENABLE (Pin 1 High)	DISABLE (Pin 1 Low)
Output	Frequency Output	High Z State
Oscillator	Oscillates	Oscillates
Current	Normal	Lower than normal

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SPECIFICATIONS TABLE *Parameters listed are at T_{AMB} 25°C unless otherwise stated.*

Parameter	Symbol	Units	Tightest	Standard	Maximum	Conditions/Comments
Frequency Stability		ppm	±75	±100	±150	-40° to +105°C
		ppm	±25	±50	±100	-40° to +85°C
Ageing		ppm		±5		First year, dependant upon frequency
Calibration Tolerance		ppm	±25	±50	±100	@25°C, other tolerances available
Frequency Tolerance (Total)		ppm	±25	±50	±100	-40° to +85°C
LVDS Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions/Comments**
Output Differential Voltage	V_{OD}	mV	247	355	454	
VDD Magnitude Change	ΔV_{OD}	mV	-50		50	
Output High Voltage	V_{OH}	V		1.4	1.6	RL = 100Ω (See Figure 2.)
Output Low Voltage	V_{OL}	V	0.9	1.1		
Offset Voltage	V_{OS}	V	1.125	1.2	1.375	
Offset Magnitude Change	ΔV_{OS}	mV	0	3	25	
Power-off Leakage	I_{OXD}	µA		±1	±10	V_{OUT}=V_{DD} or GND (V_{DD}=0V)
Short Circuit Current (Output)	I_{OSD}	mA		-6	-8	
Rise Time (Differential Clock)	t_R	ns	0.2	0.7	1	RL = 100Ω 20% to 80% (See Figures 3 & 4)
Fall Time (Differential Clock)	t_F	ns	0.2	0.7	1	
Supply Current (Outputs Loaded)	I_{DD}	mA		30*	80	*Typical for 125MHz
Duty Cycle (Output Clock)		%	40		60	@1.25V
LVPECL Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions/Comments**
Output High Voltage			V_{DD} -1.025			RL = 50Ω to (V_{DD} - 2V) See Figure 5.)
Output Low Voltage					V_{DD} -1.620	
Rise Time	t_R	ns		0.6	1.5	20% to 80% (See Figure 6)
Fall Time	t_F	ns		0.5	1.5	20% to 80% (See Figure 6)
Supply Current (Outputs Loaded)	I_{DD}	mA			100	
Duty Cycle (Output Clock)		%	40		60	@V_{DD} -1.3V
CMOS Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions/Comments**
Short Circuit Current		mA		±50		
Output Drive Current	I_{OH}	mA	20	25		V_{OH} = V_{DD} -0.4V, V_{DD} = 3.3V
(CMOS)	I_{OL}	mA	20	25		V_{OL} = 0.4V, V_{DD} = 3.3V
Rise/Fall Time (CMOS)	$t_R t_F$	ns		1.5		10% to 90% 3.3V, 15pF
Output Load (CMOS)	CL	pF			15	(See Figure 1)
Supply Current (Outputs Loaded)	I_{DD}	mA			40	200MHz maximum
Duty Cycle (Output Clock)	%		40		60	@50% V_{DD}
Timing Jitter						
Jitter (Integrated) (LVDS)		ps		0.3	0.4	125MHz (12kHz to 20MHz RMS)
Jitter (Period) (LVDS)		ps		2		125MHz (10,000 cycles RMS)

Phase Noise - 125MHz	Offset Frequency	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz
Typical (LVDS)	dBc/Hz	-85	-110	-133	-143	-148

HOW TO ORDER DFXO OSCILLATORS

DFXO C 4 T SM3 - 300.0M , 50 / 50 - /I

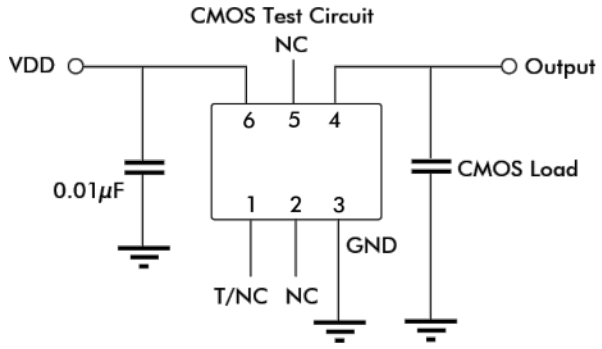
C	4	T	SM3	300.0M	50	50	/I
Output Type C = CMOS D = LVDS P = LVPECL	Supply Voltage 2 = 2.5V 4 = 3.3V	Enable/Disable Option T or N	Terminations Blank = SM1 =Gold plated, (Pb free) SM3 = Solder Dipped SM5 = Solder Dipped (Pb free)	Frequency M = MHz	Calibration Tolerance @25° (in ppm)	Frequency Stability over Temp. Range (in ppm)	Temp. Range C = -10° to +70°C I = -40° to +85°C E = -40° to +105°C S = Customer specified

ALTERNATIVELY

-- / -- / 100 /I

--	--	100	/I
		Total Frequency Tolerance (±ppm)	Temp. Range C = -10° to +70°C I = -40° to +85°C E = -40° to +105°C S = Customer specified

Figure 1.



Note: a 0.1µF bypass capacitor between VDD and GND pins as close as possible is recommended to minimise power supply line noise.

Figure 2.

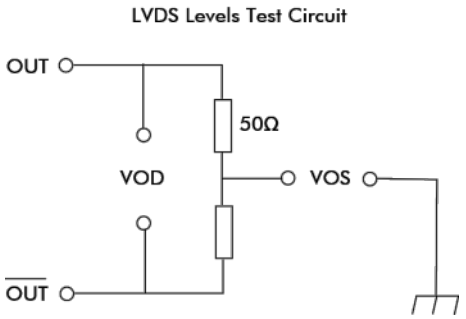


Figure 3.

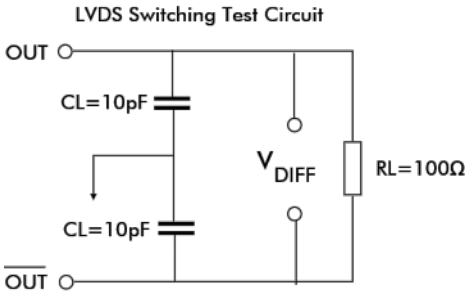


Figure 4.

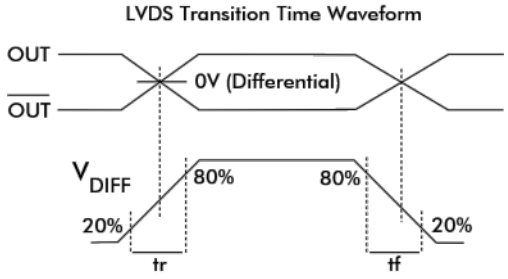


Figure 5.

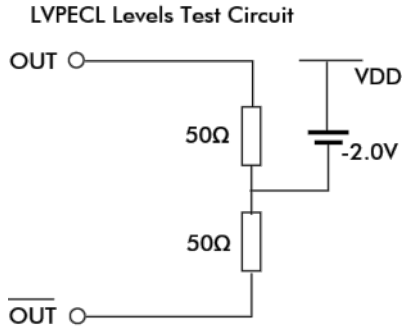
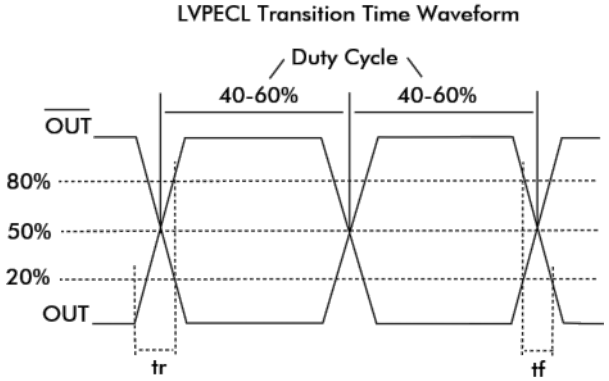


Figure 6.



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